

Table 4: Results of our analytical analog placement framework (NLP).

Design	NLP						Device layer-aware NLP					
	area (μm^2)		HPWL (μm)		run-time (s)		area (μm^2)		HPWL (μm)		run-time (s)	
	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.
opamp	2973	1	753	1	17.1	1	2370	0.80	498	0.66	10.9	0.64
g_m -C integrator	182	1	73	1	1.2	1	175	0.96	60	0.83	1.2	1.00
CTDSM	57455	1	3129	1	6.5	1	56060	0.98	2580	0.82	6.5	1.00
average		1		1		1		0.91		0.77		0.88

Table 5: Results of MILP-based placement with quality matching (MILP-Q), and run-time matching (MILP-R) our framework without device layer-awareness (NLP).

Design	NLP						MILP-Q						MILP-R					
	area (μm^2)		HPWL (μm)		run-time (s)		area (μm^2)		HPWL (μm)		run-time (s)		area (μm^2)		HPWL (μm)		run-time (s)	
	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.	actual	norm.
opamp	2973	1	753	1	17.1	1	3295	1.11	714	0.95	607.2	35.57	4181	1.41	927	1.23	20.2	1.19
g_m -C integrator	182	1	73	1	1.2	1	187	1.03	69	0.95	20.7	17.21	184	1.01	77	1.06	5.7	4.73
CTDSM	57455	1	3129	1	6.5	1	57960	1.01	3611	1.15	20.5	3.16	64472	1.12	3443	1.10	10.5	1.62
average		1		1		1		1.05		1.02		18.65		1.18		1.13		2.51

Table 6: Global routing (GR) results for the proposed analytical placement framework (NLP).

wirelength (μm)	NLP + GR		Device layer-aware NLP + GR	
	actual	norm.	actual	norm.
opamp	839	1	617	0.74
g_m -C integrator	89	1	79	0.89
CTDSM	3591	1	3034	0.84
average		1		0.82

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